SPI NAND Robust Read Method

Author: Mohammad Nada
Associated Part Family: S35ML0xG3

This application note, AN223239, details a safe flow for SPI NAND device host read operation using a "double check" method for status register ready status. This application note is applicable to SPI NAND family

1 Background

The NAND Flash memory is designed with a powerful internal ECC engine.During a READ operation, the page data is read from the array to the page buffer, where the ECC code is calculated and compared with the value read from the array. if errors are detected, the error is corrected in the page buffer . The ECC status register bits indicates the status of the error correction. When the ECC operation is complete, it sets the OIP signal in the C0h register to inform the host that the data is ready to be read. For a safe system operation, the host needs to check if the device is ready. In this application note, it is recommended to have a “Double checking device readiness” method.

2 Status Register

SPI NAND devices have a read only 8-bit status register (Table 1) that software can read during the device operation. The status register can be read by issuing the GET FEATURES (0Fh) command,followed by the feature address (C0h). The status register will output the status of the operation and whether the device is ready.

Table 1: Feature Address C0h (Status Register R Only)

Bit	Symbol	Parameter	Default	Description
7	Reserved	Reserved	0	
6	Reserved	Reserved	0	
5	ECCS1	ECC status register[1:0][1,2]	0	11 = 5-6 errors (Rewrite recommended) 10 = 3-4 errors corrected 01 = 1-2 errors corrected 00 = Normal
4	ECCS0		0	
3	P_Fail	Program fail	0	1: Program failure occurred 0: Operation passed
2	E_Fail	Erase fail	0	1: Erase Failure occurred 0: Operation passed
1	WEL	Write enable latch	0	1: Write Enabled 0: Write Disabled
0	OIP	Operation in progress	0	1: Device is busy with executing commands: Reset, Program Execute, Page Read, Block Erase 0: Device is ready

1: SR [5:4] defines the number of corrections.

2: 11 can be used as uncorrectable.

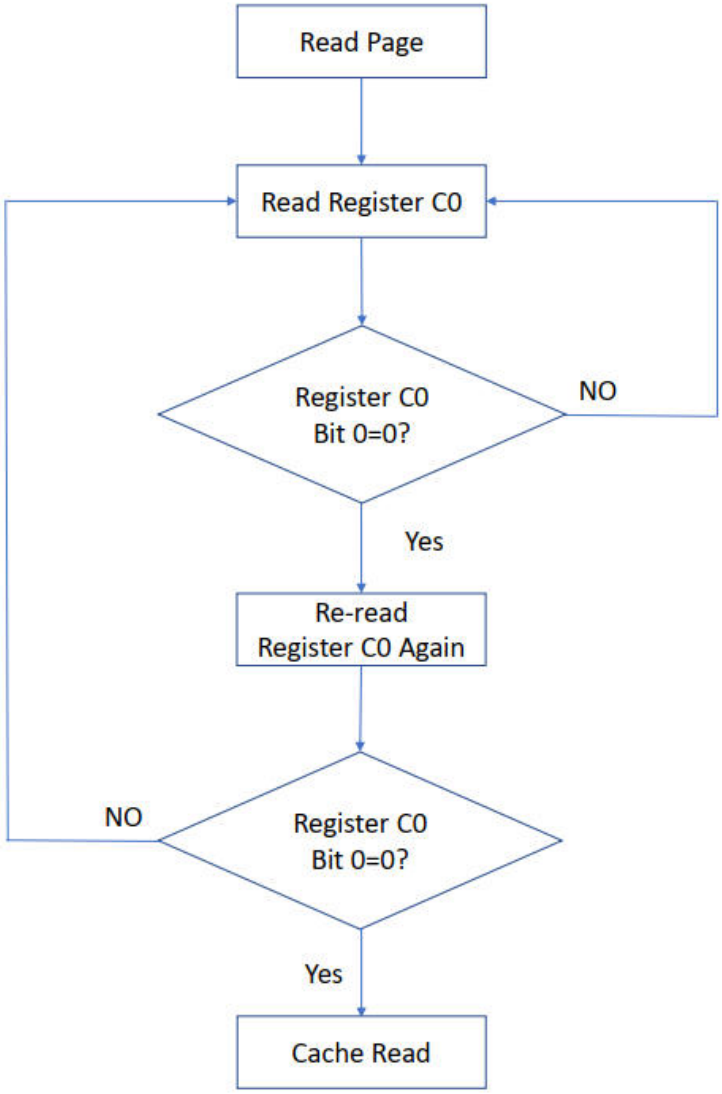
3: A Program and Erase fails include a block being protected (Array blocks + OTP) for 1Gb/2Gb densities

A Program fail does not include OTP block for 4Gb density

3 Status Register consecutive reads

Under normal operation, the host continues polling the status register till Bit 0 of the register is "0" indicating that the device is ready. Once bit 0 of the status register is ready, it is highly recommended that the host reads the status register again to insure that the device is ready and the host can resume sending new commands. The two consecutive reads of the status register guarantee that the device is ready and avoid any bus contention issues if the host resumes sending commands pre-maturely.
The recommended flow is shown in the flow chart of Figure 1.

Figure 1: Status Register Consecutive Reads Flow Chart



4 References

- SPI- S35ML01/02/04 G3 1/2 Gb, 3 V, 2K Page Size, x8 I/O SLC NAND Flash Memory for Embedded, Datasheet, Specification Number 002-19205

- Linux 5.18- SPI NAND Read Flow

  http://www.skyhighmemory.com/download/softwareTools/linux-5.18-mtd-nand-spi-core-read-page-wait.patch.zip

5 Document History

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**		MNAD	09/21/2022	New Application Note